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A PARALLEL MULTIPLIER AND ACCUMULATOR ARCHITECTURE

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ABSTRACT:

The Essential elements of the digital signal processing are the multiplier and multiplier and accumulator (MAC). In this paper, for high-speed arithmetic we have proposed a new architecture for multiplier and accumulator (MAC).With the earlier advances in multimedia and communication systems, real-time signal processing like audio and video/image processing are increasingly high in demanded. The performance can be improved by combining multiplication with accumulation and by dividing a hybrid type of carry save adder (CSA). The overall performance will be elevated, since the accumulator that has the largest delay in MAC was merged into CSA. In order to increase the bit density of the operands, the proposed CSA tree uses 1's-complement-based on radix-2 modified Booth's algorithm (MBA) and has the modified array for the sign extension. In order to decrease the number of the input bits of the final adder CSA propagates the carries to the least significant bits of the partial products and generates the least significant bits. Instead of the output of the final adder, the proposed MAC accumulates the intermediate results in the type of sum and carry bits, which made it possible to optimize the pipeline scheme to improve the performance. In the similar clock frequency the proposed MAC shows the superior properties of the standard design in many ways and performance twice as much as in previous research. The high performance can be adapted by proposed MAC to various fields such as the signal processing areas.

Keywords: Multiplier and accumulator, Carry save adder, Booth algorithm, Standard design.

INTRODUCTION

A series of repeated additions can be considered as multiplication. The number to be added is multiplicand, and the number of times that it is added is the multiplier, and the result is the product. Partial product can be generated by each step of addition. The operand usually contains the same number of bits in most of the computers. The essential elements of the digital signal processing are the multiplier and multiplier and accumulator (MAC) and filtering, convolution, and inner products. Most of the digital signal processing methods use nonlinear functions such as discrete cosine transforms (DCT) or discrete wavelet transforms (DWT). The speed of the multiplication and addition arithmetic determines the execution speed and performance of entire calculation for high-speed multiplication, the modified radix-4 Booth's algorithm (MBA) is commonly used by repetitive application of multiplication and addition. However, due to the long critical path for multiplication this cannot completely solve the problem.ral, a multiplier uses Booth's algorithm and array of full adders (FAs), or Wallace tree instead of the array of FAs.. In this paper, a new architecture for a high-speed MAC is proposed. In this MAC, the computations of multiplication and accumulation are combined and

a hybrid-type CSA structure is proposed to reduce the critical path and improve output rate. It uses MBA algorithm based on 1's complement number system. The density of the operands is increased by using modified array structure for the sign bits. To reduce the number of bits in the final adder, a carry look-ahead adder (CLA) is inserted in the CSA tree. In order to increase the output rate by optimizing the pipeline efficiency, intermediate calculation results are accumulated in the form of sum and carry instead of the final adder outputs.accumulation are combined and a hybrid-type CSA structure is proposed to reduce the critical path and improve output rate. It uses MBA algorithm based on 1's complement number system. A modified array structure for the sign bits is used to increase the density of the operands. A carry look-ahead adder (CLA) is inserted in the CSA tree to reduce the number of bits in the final adder. In addition, in order to increase the output rate by optimizing the pipeline efficiency, intermediate calculation results are accumulated in the form of sum and carry instead of the final adder outputs.

OVERVIEW:

A multiplier can be divided into three operational steps. The first is radix-2 Booth encoding in which a partial product is generated from the multiplicand and the multiplier. The second d is adder array or partial product compression to add all partial products and convert them into the form of sum and carry. The last is the final addition in which the final multiplication result is produced by adding the sum and the carry. If the process to accumulate multiplied results is included, a MAC consists of four steps, The inputs for the MAC are to be fetched from memory location and fed to the multiplier block of the MAC, which will perform multiplication and give the result to adder which will accumulate the result and then will store the result into a memory location.

REQUIREMENTS:

The design specifications for the parallel multiplier include the general requirements for designing the parallel multipliers and special requirements for implementing the 8
by 8 bit multiplier. Both of them are described as follows.

Multiplicand: n-bit number

Multiplier: n-bit number.

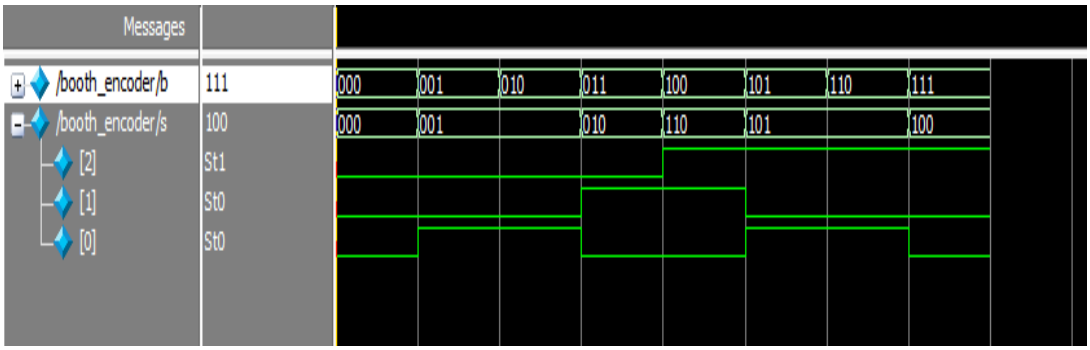
Product: 2n-bit number.

MULTIPLIER ARCHITECTURE:

However, for high-speed applications, the parallel multiplier is one of the best solutions. In general, the architecture of a parallel multiplier consists of the following parts: partial product generator (PPG), partial product reduction tree (PPRT), and final addition. Each part can be implemented by using various architectural choices. Figure 3.1 shows the architecture of the parallel multiplier that has been widely applied for the large multiplier. This architecture consists of modified Booth encoder, partial product generator, Wallace tree that is also called partial product reduction tree, and vector merging adder (VMA).

PROJECT SCOPE:

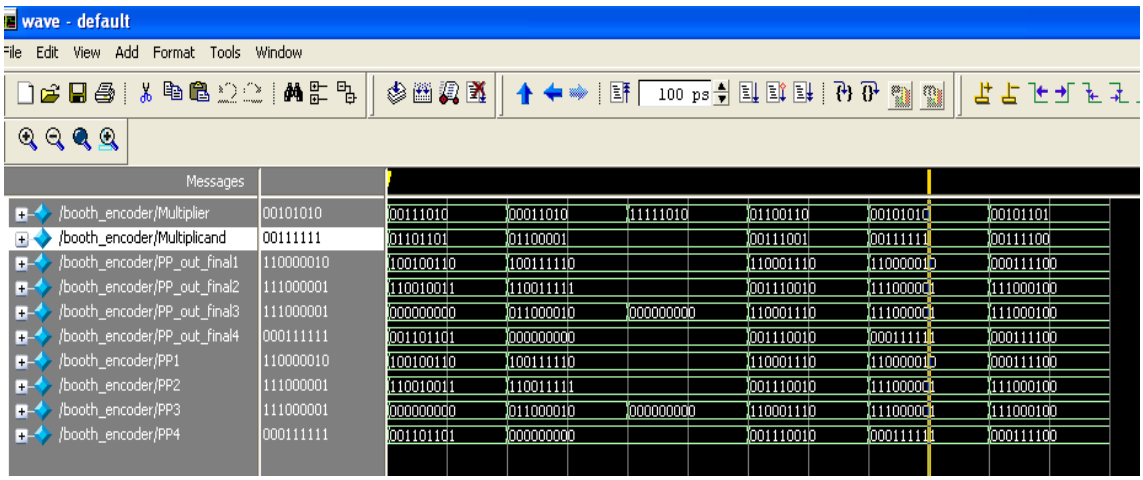
Booth Encoder:3 bit group of multiplier applier applied on booth encoder, It generates booth



signals (0, +1, +2,-1,-2). Here S[2] is sign bit and s[0:1] is signal value.

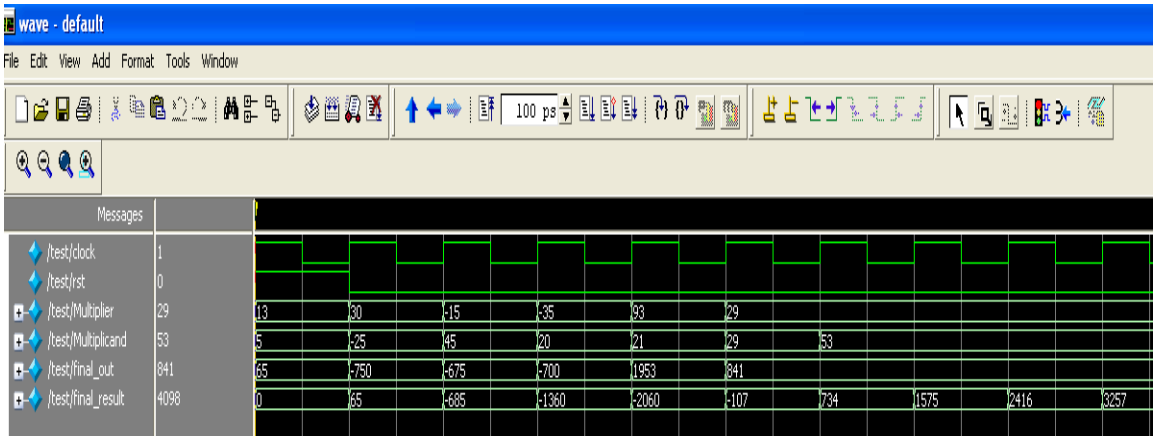
Partial Products:

Simulation results of partial products are shown below



MAC:

Simulation results of MAC. For every rising edge clock final output will come.



RTL Schematic of MAC:

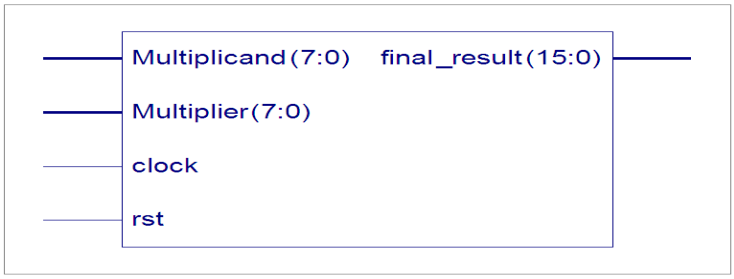


Fig4.1 RTL schematic for MAC

Blocks inside the developed top level MAC design

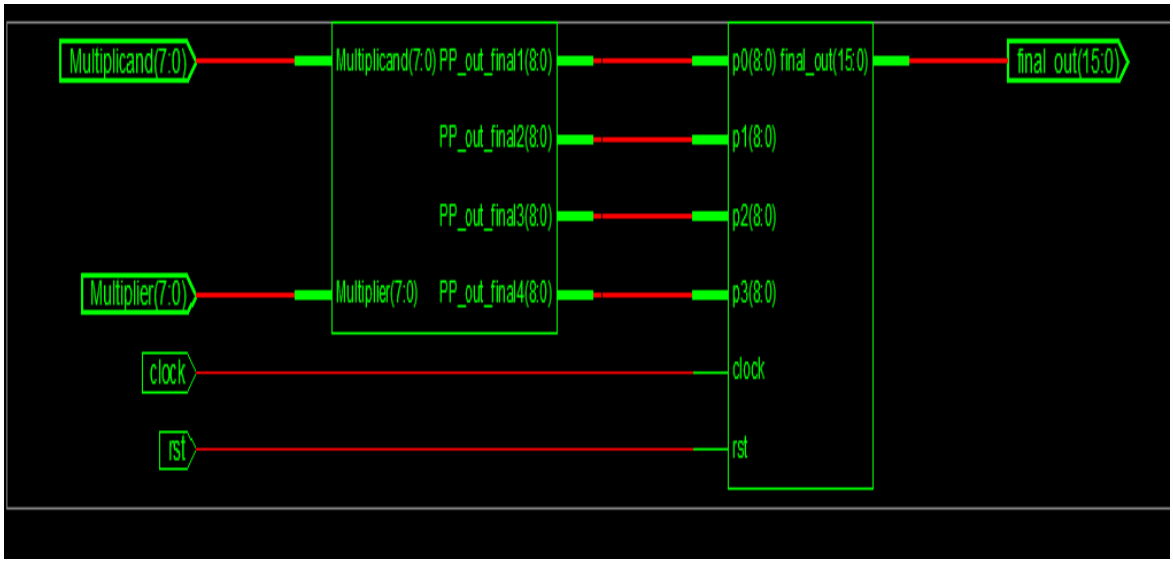


Figure 4.2 Top Level MAC Design

CONCLUSION:

In this paper, a new MAC architecture to execute the multiplication-accumulation operation, which is the key operation, for digital signal processing and multimedia information processing efficiently, was proposed. By removing the independent accumulation process that has the largest delay and merging it to the compression process of the partial products, the overall MAC performance has been improved almost twice as much as in the previous work.

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