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Performance Evaluation of Low Power Adder in 32nm CMOS Technology

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ABSTRACT:

In real time applications, the adder circuit is a basic building block in Digital Signal Processor, microprocessor, microcontroller and data processing units. Addition is one of the fundamental operations in arithmetic circuits. The adder cells must be designed in such a way as it reduces power and delay. In this paper, existing adders are surveyed and analyzed intensively. Saving power in adders would reduce the power consumption significantly at the chip level and performance of a device will be enhanced. To obtain efficient full adder the proposed hybrid adder is introduced. The proposed low power adder is suitable for obtaining the low power consumption, less propagation delay and efficient power delay product. All simulations are performed on 32nm CMOS technology in Synopsys HSpice.

Keywords: Shannon adder, Hybrid adder, CPL, MCIT, Low power adder, Average Power.

[I] INTRODUCTION

Due to rapid growth in portable electronics and communication systems like laptops, mobile phones, PDA's, etc., the low power microelectronic devices has become very important in today's world [3]. In fact, Low-power VLSI chips have emerged in high demand for designing any sub system. With an increase in complexity of VLSI systems and amount of power available in certain systems like cell phones and digital cameras, minimizing power consumption is essential. All battery operated mobiles and implanted devices require maximum battery life [2]. With the advancement of VLSI technology, many computing intensive applications such as multimedia processing, digital communication can now be realized in hardware to either speed up the operation or reduce the power/energy consumption. The essence of the digital computing lies in the design of full adder. The design criteria of a full adder are usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many functional units such as multiplier and compressor [4], [6]. Two other important, yet often conflicting, design criteria are power consumption and delay.

Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI circuits and systems such as comparators, parity checkers, application-specific DSP architectures and microprocessors. In most of these systems, the adder is part of the critical path that determines the overall performance of the system [6]. Enhancing the performance of Full adder can significantly affect the system performance. The performance of a full adder circuit depends on the type of the design style used for implementation as well as the logic function realized using the particular design style. So, it is very important to choose the adder topology to yield the desired performance.

This Paper is organized as follows: In section 2, Overview of full adder cell is presented. In section 3, existing Shannon adder and hybrid adder is described. In section 4, proposed hybrid adder is given. In section 5, simulation results and performance analysis are presented and finally in section 6, concludes the paper.

[II] FULL ADDER CELL

Generally, a full adder is defined as a logic cell that performs an addition operation on three one-bit binary numbers. The full adder produces two-bit output which is carry and sum. Full adder cell is implemented in low power and high performance data path circuit. The full adder consists of three input signals, i.e., A, B and Cin (Carry in) and two output signals sum and carryout which is shown in Fig.1.
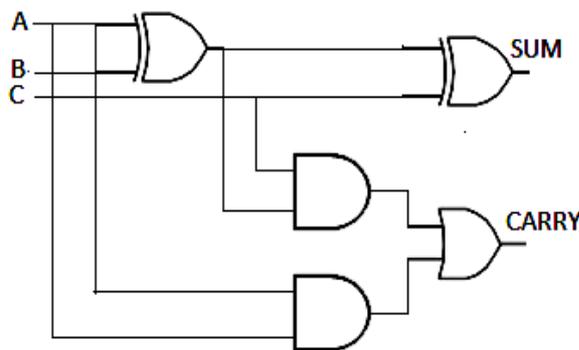
Fig: 1. Logic diagram of a Full Adder

There are various design techniques for implementation of full adder circuit is available [7]. Some of them are Multiplexing Control Input Technique (MCIT), Gate Diffusion Input technique (GDI), Technique based on static CMOS Inverter, Multi-threshold CMOS circuit technique (MTCMOS).

[III] EXISTING SYSTEM

Adders are the basic building module in all multipliers, filters and MAC unit of DSP processor. Hence employing fast adders plays a key role in the performance of the entire all data path circuits. In this section existing adder cells are described and analyzed.

3.1. Shannon Adder

The Shannon adder is designed with the Complementary Pass Transistor Logic (CPL) technique and the multiplexing control input technique (MCIT) for both sum and carry operations. The sum operation is designed based on equation (1) where two XOR logic gates are used, since pass-transistor logic is advantageous in constructing XOR logic gates. On the other hand, the carry circuit is designed with respect to equation (2). By combining the sum and carry circuits, the XOR gate in the carry operation can be omitted, and both circuits can share the common term, a xor b, in the sum operation.

$$\text{Sum} = A \text{ xor } B \text{ xor } C \qquad \text{... (1)}$$
$$\text{Cout} = (A \text{ xor } B) \text{ Cin} + AB \qquad \text{... (2)}$$

The inputs A, A's complement (A'), B, and B's complement (B') are fed as inputs to the pass transistors and form an XOR logic gate. These four inputs construct an XOR logic operation in transistor level, which is designed with two transistors. To reduce the number of transistors, the output of the XOR gate (A xor B) is fed through an NOT gate from the differential node to the pass transistors as a control input. On the other hand, Cin is treated as variable input, which is fed through the pass transistor's source terminal. At this stage, the functionality of the circuit is equivalent to sum operation, sum A xor

B xor C, and six transistors are used. As mentioned previously, the number of transistors in the carry operation can be optimized by taking A xor B as the input from the sum operation circuit AND with Cin to produce the operation equivalent to (A xor B) Cin, which only uses another two transistors. Meanwhile, the inputs A, A', B, and B' are fed in to pass transistors to produce AND logic gate, which represents the AB operation in Equation (2). The outputs of both (A xor B) Cin and AB are used as multiplexing inputs to sum both terms with the OR gate operation. The transistor count can be minimized by modifying the OR gate at the last stage of the carry equation. This is achieved by removing the inverter and transistor fed by the inverter. Markovic's full adder circuit has 22 transistors. At an earlier point, 3 transistors were omitted in this design and the number of transistors of the full adder cell was reduced to 17 as shown in Fig.2 after applying the redundant technique [12].
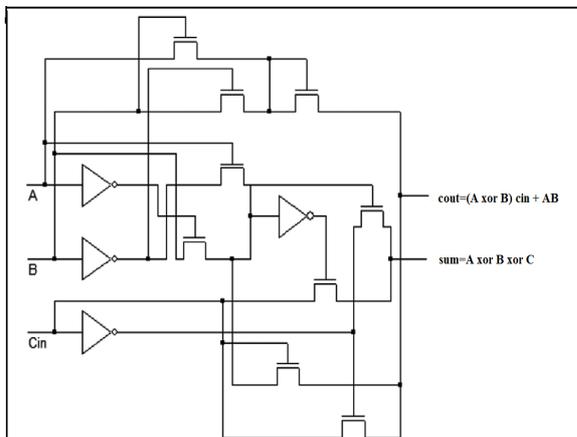

Fig: 2. Shannon Adder

3.2 Hybrid Adder

A Hybrid adder is a combination of 14T sum and modified Shannon carry. It consists of 12 transistors. The width is optimized by transistor sizing to bring the better power consumption without degrading the delay. For further improvement in terms of power, delay and driving capability Hybrid full adder circuit is implemented as shown in Fig.3. Hybrid full adder

circuits provide good driving capability and better power delay performance [7].
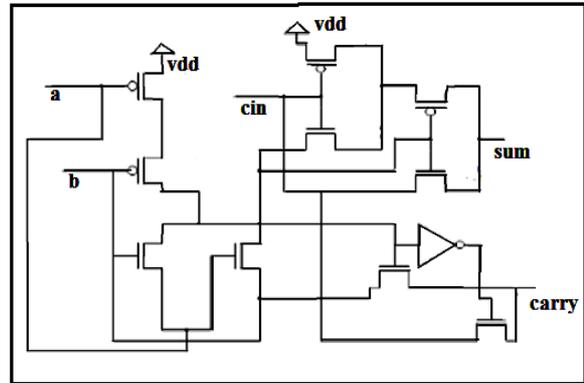

Fig: 3. Hybrid Adder

[IV] PROPOSED SYSTEM

A Hybrid adder is proposed by modifying the existing hybrid adder. In existing system, inverter is used in the design; the modified design doesn't consist of inverters since they are Power hungry components. The nMOS transistor that needs the inverted input has been replaced by pMOS transistor as shown in Fig.4. Hence, overall area, power consumption and switching activities are reduced in which the design becomes prominent for low power applications.
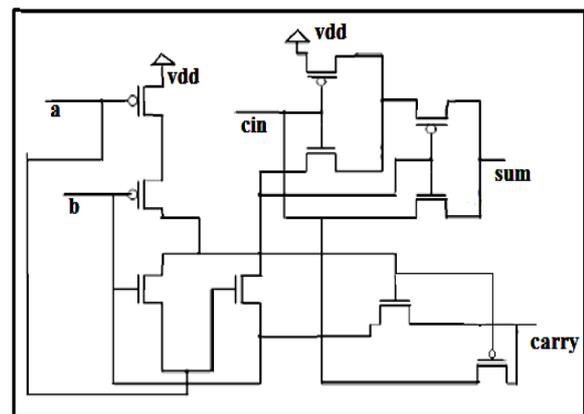

Fig: 4. Proposed Hybrid adder

[V] RESULTS AND DISCUSSION
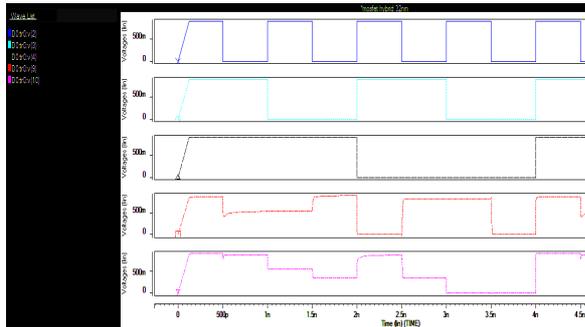### 5.1 Transient analysis

To evaluate the performance of Shannon adder, hybrid adder and proposed hybrid adder circuits

discussed in this paper are designed in 32nm CMOS Technology. All simulations are performed in HSpice simulation tool. Fig's 5, 6 and 7 represent the simulation results of the above mentioned circuits.
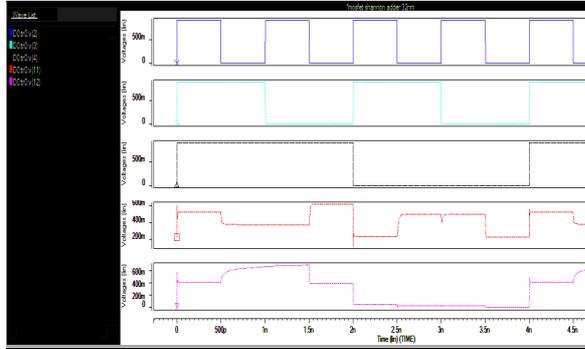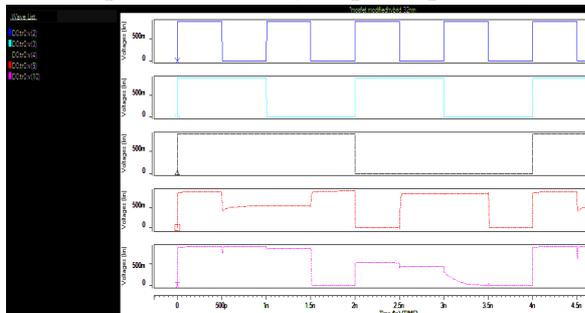

Fig: 5. Existing Shannon Adder simulation output

Fig.5 depicts the transient analysis of Shannon adder where V(2), V(3), V(4) represents the inputs and V(11) represents the sum output and V(12) represents the carry output respectively.

Fig: 6. Existing Hybrid adder simulation output

Fig.6 describes the transient analysis of Hybrid adder where V(2), V(3), V(4) represents the inputs and V(11) represents the sum output and V(12) represents the carry output respectively.

Fig: 7. Proposed Hybrid adder simulation output

Fig.7 explains the transient analysis of proposed hybrid adder where V(2), V(3), V(4) represents the inputs and V(11) represents the sum output and V(12) represents the carry output respectively.

5.2 Performances analysis

The performance parameters compared are average power, delay and power delay product.

Designs	Shannon Adder	Hybrid Adder	Proposed Hybrid Adder
Average power(µW)	$2.646e^{-05}$	$1.460e^{-05}$	$1.116e^{-05}$
Delay(s)	$520.53e^{-12}$	$496.79e^{-12}$	$267.55e^{-15}$
Power delay product(J)	$1.3773e^{-14}$	$7.2531e^{-15}$	$2.9858e^{-18}$

Table: 1. Comparison of existing and proposed full adder in 32nm CMOS technology

In CMOS design, comparing the power, delay and power delay product of proposed Hybrid Adder design to existing adders the proposed Adder is efficient than the existing Adder as shown in Table .1.

[VI] CONCLUSION

In this paper, Hybrid full adder is proposed for low power DSP application. The proposed circuit uses full adder with 10T, Modified Shannon circuits and hybrid adder. The existing two adders and proposed hybrid full adder circuits are implemented and simulated in HSpice in 32nm CMOS Technology .The power, delay and PDP values of all the full adder circuits are analyzed. It is observed from the simulated results that the proposed circuit has the minimum Delay, less Power Consumption and reduced power delay product. It is noted that proposed Hybrid adder has the better power consumption compared with existing Hybrid adder and delay performance is

good in the proposed circuit. Hence the proposed Hybrid adders can be utilized for low power high performance applications as a future work.

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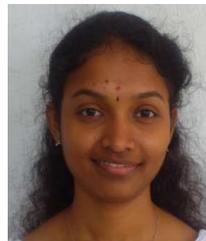
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